Applicant thanks the Examiner for the allowance of Claim 15.

In response to the objection to the drawings, Applicant submits herewith corrected Figures 9 and 10. Applicant respectfully submits that the modifications to the drawings do not add any new matter, but simply clarify matters set forth in the originally-filed application. Accordingly, Applicant respectfully requests that this objection be reconsidered and withdrawn.

The rejection of Claims 1-4, 8-10, 14, and 16-18 under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (U.S. Patent No. 4,970,694, hereinafter referred to as "Tanaka") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 1-4, 8-10, 14, and 16-18 are patentable over Tanaka.

Applicant notes that although paragraph 5 of the Office Action recites that Claims 1-5, 9-11 and 15-17 are rejected, the paragraphs that follow in the Office Action support the rejection being to Claims 1-4, 8-10, 14 and 16-18. Accordingly, Applicant has addressed this rejection with respect to Claims 1-4, 8-10, 14 and 16-18.

Claim 1 recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level. An inverter chain contains not less than one inverter. A metal-oxide-semiconductor capacitor, known as a MOS capacitor, has a single transistor per stage of the inverter chain connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter. Each stage is tied alternately

to one of a power voltage source and a ground voltage source. The MOS capacitor is represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage. Claims 3 and 4 depend from Claim 1.

Claim 2 recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level. An inverter chain contains not less than one inverter. A metal-oxide-semiconductor capacitor, known as a MOS capacitor, has a single transistor per stage of the inverter chain connected to an output section of the inverter and exhibits changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage. Each stage is tied alternately to one of a power voltage source and a ground voltage source. The MOS capacitor is represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage. Claims 9 and 10 depend from Claim 2.

Claim 8 recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level. An inverter chain contains not less than one inverter. A metal-oxide-semiconductor capacitor, known as a MOS capacitor, is connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter. The MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by a p-MOS transistor whose source and drain are connected to a node that changes a logic level of a logic signal from a high level to a low level, and whose gate is fixed at a ground potential.

Claim 14 recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level. An inverter chain contains not less than one inverter. A metal-oxide-semiconductor capacitor, known as a MOS capacitor, is connected to an output section of the inverter and exhibits changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage. The MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by a p-MOS transistor whose source and drain are connected to a node that changes a logic level of a logic signal from a high level to a low level, and whose gate is fixed at a ground potential.

Claim 16 recites a method for delaying a logic signal having two logic levels consisting of a low level and a high level. A metal-oxide-semiconductor capacitor disposed on a transmission path of a logic signal is set to an off-state in an initial stage. The metal-oxide-semiconductor capacitor is changed to an on-state from the off-state according to a logic level of the logic signal. The metal-oxide-semiconductor capacitor is represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage. Claim 17 depends from Claim 16.

Claim 18 recites a delay circuit comprising a plurality of cascading gate circuits and a plurality of MOS capacitors connected to the output sections of said gate circuits. A the MOS capacitors are connected so as to turn from the off-state to the on-state when the logic signal having the logic level targeted for delay is input into the head gate circuit among the cascading gate circuits. Each of the MOS capacitors is represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage.

Tanaka discloses supplying a first chip enable signal for determining the operation timing of a memory chip to a first chip enable input circuit. Tanaka's Figure 7 discloses a first chip enable input circuit 1 that includes CMOS inverters 31-39, MOS capacitors 40-42 and CMOS NAND gate 43. Signal CE1 is supplied to one input terminal of the NAND gate 43 via inverters 31 to 33 The output of inverter 33 is supplied to the other input terminal of the NAND gate 43 via delay circuit 30 formed of inverters 34 and 36 and capacitors 40 to 42. The output of NAND gate 43 is supplied to a second chip enable circuit 2 via inverters 37 to 39. (Col. 3, Line 60-Col. 2, Line 3; Figure 7).

The Office Action states that Tanaka does not disclose that the MOS capacitor is represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage.

The Office Action further states that Applicant discloses in the specification that is it well known that p-MOS (or n-MOS) transistors having their gate connected to the output section of the inverter and their source and drains tied to a source voltage can be replace with n-MOS (or p-MOS) transistors having their source and drains tied to the output section of the inverter and their gates tied to a source voltage. Applicant respectfully submits that the Office Action has cited no section or location as to where this is set forth in Applicant's specification. Applicant respectfully requests specific information regarding what portion or section of Applicant's specification is being relied upon to support the statement that Applicant's specification discloses that the foregoing teaching is well-known. Applicant respectfully submits that there is no mention in Applicant's BACKGROUND of such teaching being well-known such that the Office Action may rely upon such as a basis for this rejection. Applicant's Background section

discloses in Figure 16 an arrangement in which the gate terminals of n-MOS transistors JN1-JN4 are connected to the output section of inverters and the source and drain of the n-MOS transistors JN1-JN4 are connection to ground in which JN1-JN4 form MOS capacitors. (page 1, line 10-page 2, line 5).

Applicant's specification in the DESCRIPTION OF THE PREFERRED EMBODIMENTS section discusses different embodiments of Applicant's claimed invention. One embodiment of Applicant's invention is shown in Figure 3 in which the gate terminals of the n-MOS transistors N31 and N32 are fixed at a source voltage and the gate terminals of the p-MOS transistors are fixed to ground. (See DESCRIPTION OF THE PREFERRED EMBODIMENTS section, page 19, line 4-page 20, line 3). Applicant's specification in the DESCRIPTION OF THE PREFERRED EMBODIMENTS at page 20, line 4-page 21, line 1 further states that the p-MOS transistors P21, P22 and the n-MOS transistors N31 and N32 of Figure 1B may be replaced with n-MOS transistors N31 and N32 and the p-MOS transistors P31 and P32 in which the source and drain of the MOS transistors are connected to the output section of each inverter and the gate is fixed at the source voltage or ground potential.

In view of the foregoing, Applicant respectfully submits that the only mention of an arrangement in which the gate of a transistors is fixed at a source voltage or ground potential is set forth in the DESCRIPTION OF THE PREFERRED EMBODIMENTS section which describes embodiments of Applicant's claimed invention.

Further to the above, Applicant respectfully submits that Applicant's Claim 1 is patentable over Tanaka, taken alone or in combination with teachings from Applicant's

Background section of the specification, in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: an inverter chain containing not less than one inverter; and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage,*** as set forth in Applicant's Claim 1. The Office Action states that Tanaka does not disclose that the MOS capacitor is represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage. Applicant further submits that the only teaching in Applicant's specification of a MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage is in the description of embodiments of Applicant's claimed invention. Applicant's Background is silent regarding any disclosure of a MOS capacitor is represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage. Accordingly, Applicant respectfully submits that Tanaka, and Tanaka in combination with teachings from Applicant's Background section of the specification, do not disclose, teach or suggest the feature of ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: ... a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain ..., said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage,*** as set forth in Applicant's Claim 1.

For reasons similar to those set forth regarding Applicant's Claim 1, Applicant's Claim 2 is patentable over Tanaka, and Tanaka in combination with teachings from Applicant's Background section, in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises: an inverter chain containing not less than one inverter; and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter and exhibiting changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage***, as set forth in Applicant's Claim 2.

For reasons similar to those set forth regarding Applicant's Claim 1, Applicant's Claim 8 is patentable over Tanaka, and Tanaka in combination with teachings from Applicant's Background section, in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: an inverter chain containing not less than one inverter; and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by a p-MOS transistor whose source and drain are connected to a***

node that changes a logic level of a logic signal from a high level to a low level, and whose gate is fixed at a ground potential, as set forth in Applicant's Claim 8.

For reasons similar to those set forth regarding Applicant's Claim 1, Applicant's Claim 14 is patentable over Tanaka, and Tanaka in combination with teachings from Applicant's Background section, in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises: an inverter chain containing not less than one inverter; and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, connected to an output section of the inverter and exhibiting changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by a p-MOS transistor whose source and drain are connected to a node that changes a logic level of a logic signal from a high level to a low level, and whose gate is fixed at a ground potential,*** as set forth in Applicant's Claim 14.

For reasons similar to those set forth regarding Applicant's Claim 1, Applicant's Claim 16 is patentable over Tanaka, and Tanaka in combination with teachings from Applicant's Background section, in that the references neither disclose nor suggest ***a method for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising the steps of:(a) setting a metal-oxide-semiconductor capacitor disposed on a transmission path of a logic signal to an off-state in an initial stage; and (b) changing the metal-oxide-semiconductor capacitor to an on-state from the off-state according to a logic level of the logic signal, said metal-oxide-semiconductor capacitor represented by at least one transistor whose***

gate is fixed at one of a ground potential and a source voltage, as set forth in Applicant's Claim 16.

For reasons similar to those set forth regarding Applicant's Claim 1, Applicant's Claim 18 is patentable over Tanaka, and Tanaka in combination with teachings from Applicant's Background section, in that the references neither disclose nor suggest ***a delay circuit comprising a plurality of cascading gate circuits and a plurality of MOS capacitors connected to the output sections of said gate circuits, wherein: all the MOS capacitors are connected so as to turn from the off-state to the on-state when the logic signal having the logic level targeted for delay is input into the head gate circuit among said cascading gate circuits, each of said MOS capacitors represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage***, as set forth in Applicant's Claim 18.

In view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

The rejection of Claims 5 and 11 under 35 U.S.C. 103(a) as being unpatentable over Tanaka and Hattori (U. S. Patent No. 5,459,424, hereinafter referred to as "Hattori") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 5 and 11 are patentable over the references, taken separately or in combination.

Applicant's Claim 5 depends from independent Claim 1. Applicant's Claim 11 depend from independent Claim 2. For reasons set forth above, Applicant's Claims 1 and 2 are neither disclosed nor suggested by Tanaka, and also neither disclosed nor suggested by Tanaka taken in

combination with Applicant's Background section of the specification. Applicant further submits that, for reasons set forth below, combining Tanaka, alone or in combination with Applicant's Background section, further in combination with Hattori also neither discloses nor suggests Applicant's Claims 1 and 2.

Hattori discloses a CMOS pulse delay circuit that can accurately delay a signal by a predetermined amount. Hattori discloses inverters that each have additional switching transistors on each end, and a voltage controlled variable resistor. The indicated portion of the reference discloses a CMOS inverter that has both an N channel and a P channel transistor located after each stage of the inverter chain. (See Figure 1; Col. 1, Lines 20-60).

Applicant's Claim 1 is patentable over the references, alone or taken in any combination, in that the references neither discloses nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: an inverter chain containing not less than one inverter; and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage,*** as set forth in Applicant's Claim 1. For reasons set forth above, Tanaka, taken alone or in combination with teachings from Applicant's Background section, neither disclose, teach, or suggest a MOS capacitor is represented by at least one transistor whose gate is fixed at one of a ground potential

and a source voltage. Hattori discloses an inverter that includes an n-type MOS transistor and a p-type MOS transistor. However, Hattori is silent on disclosing a transistor included in an inverter having a gate fixed at one of a ground potential and a source voltage. Accordingly, the references neither disclose nor suggest at least the feature of ***said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage***, as set forth in Applicant's Claim 1.

For reasons similar to those set forth regarding Claim 1, Applicant's Claim 2 is patentable over the references, taken alone or in any combination, in that the references neither discloses nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises: an inverter chain containing not less than one inverter; and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter and exhibiting changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage***, as set forth in Applicant's Claim 2.

In view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

The rejection of Claims 6-7 and 12-13 under 35 U.S.C. 103(a) as being unpatentable over Tanaka et al. (U.S. Patent No. 4,970,694) in view of Porter et al. (U.S. Patent No. 6,040,713) is

hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 6-7 and 12-13 are patentable over the cited references, taken separately or in combination.

Claim 6 depends from independent Claim 1 and Claim 12 depends from independent Claim 2. For reasons set forth above, Applicant's Claims 1 and 2 are neither disclosed nor suggested by Tanaka. For reasons set forth below, Applicant respectfully submits that combining Tanaka with Porter also neither discloses nor suggests Applicant's Claims 1 and 2.

Applicant's Claim 7 recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level. An inverter chain contains not less than one inverter. A metal-oxide-semiconductor capacitor, known as a MOS capacitor, is connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter. The MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by an n-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a source voltage.

Applicant's Claim 13 recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level. An inverter chain contains not less than one inverter. A metal-oxide-semiconductor capacitor, known as a MOS capacitor, is connected to an output section of the inverter and exhibits changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage. The MOS capacitor is a node

disposed on a transmission path of a logic signal, and is represented by an n-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a source voltage.

Porter discloses a delay path 31 in Figure 11 that includes a series of 5 inverters. The path 31 also includes n-type MOS capacitors 102, 104, 106 and 108 which are connected between the outputs of the inverters 92, 94, 96, 98 an GND. The capacitors 102, 104, 106 and 108 can be any type of suitable capacitor such as n-type MOS capacitors, metal plate capacitors, or a combination of different types of capacitors. The capacitors 102, 104, 106 and 108 may also be connected between the output of the inverters 92, 94, 96, 98 and Vcc. (Col. 6, Lines 33-45).

Applicant's Claim 1 is neither disclosed nor suggested by the references in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: an inverter chain containing not less than one inverter; and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage,*** as set forth in Applicant's Claim 1. For reasons set forth above, Tanaka, taken alone or in combination with teachings from Applicant's Background section, neither disclose nor suggest the feature of ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a***

high level, comprising: ... a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain ..., said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage, as set forth in Applicant's Claim 1. Porter appears silent with regard to any teaching, disclosure or suggestion of a MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage. Thus, Applicant respectfully submits that combining these references with Porter does not overcome the deficiencies of Tanaka, taken alone or in combination with teachings from Applicant's Background section, with respect to Applicant's Claim 1 as set forth above. Accordingly, the references neither disclose, teach or suggest the feature of ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: ... a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain ..., said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage,*** as set forth in Applicant's Claim 1.

For reasons similar those set forth regarding Claim 1, Applicant's Claim 2 is neither disclosed nor suggested by the references, taken separately or in combination, in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises: an inverter chain containing not less than one inverter; and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter and exhibiting changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source, said MOS capacitor***

represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage, as set forth in Applicant's Claim 2.

For reasons similar to those set forth regarding Claim 1, Applicant's Claim 7 is neither disclosed nor suggested by the references in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: an inverter chain containing not less than one inverter; and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by an n-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a source voltage,*** as set forth in Applicant's Claim 7.

For reasons similar to those set forth regarding Claim 1, Applicant's Claim 13 is neither disclosed nor suggested by the references, taken separately or in combination, in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises: an inverter chain containing not less than one inverter; and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, connected to an output section of the inverter and exhibiting changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage, wherein the MOS capacitor is a node disposed on a transmission path of a***

logic signal, and is represented by an n-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a source voltage, as set forth in Applicant's Claim 13.

In view of the foregoing, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
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